50HZ OPERATION OF THE K-1008 VISIBLE MEMORY AN 3

The Micro Technology Unlimited K-1008 Visible memory is designed to conform in most respects to the US televison standard of 525 (interlaced) lines and 30 frames per second. The exact figures with a 1.0mHz host processor are 260 non-interlaced lines and 60.096 frames per second. The European televison standard retains the same horizontal sweep frequency (15.75kHz) as the US but decreases the vertical sweep to 50Hz to match European utility power.

There is no physical reason why the vertical sweep frequency should be close to the power line frequency but there are economic reasons. CRT's are fairly sensitive to magnetic fields which manifest themselves by slightly deflecting the image if the field lines are parallel to the screen surface. AC magnetic fields from the power transformer (if the TV or monitor has one) are generally strong enough to cause about 1mm peak-to-peak deflection. If the sweep is the same frequency as the interferring field, the only effect is a slight distortion of the raster shape. If the frequencies are different, the distortion undulates through the raster causing swimming if the difference is small (.5 to 3Hz). For larger frequency differences the image appears to jitter, particularly when viewed at close range which is typical with computer displays. Even if the power transformer is adequately shielded or absent, ripple in the DC voltages used by the deflection circuits can cause variation in the raster width or height with the same swimming or jittering effect. Thus power frequency synchronous sweep allows the use of high radiation transformers and inadequately filtered unregulated power supplies without objectionable image degradation.

The standard MTU K-1008 Visible Memory gives good results with a high quality video monitor regardless of the power line frequency. All that is normally required is adjustment of the vertical hold control to lock into the 60Hz vertical sync signal. Any residual jitter can be reduced by shileding or moving the power transformer in the monitor. Ordinary sheet steel has rather poor shielding properties. Best results are obtained with special shielding foils. Laminations salvaged from a large transformer (such as a power distribution transformer) can also be formed into an effective shield. Moving the transformer away from the tube is usually easiest however. This can be accomplished by making an extension cable to the transformer, ideally with a plug and socket so the transformer can be unplugged when the monitor is moved. Where unregulated DC voltages are used in the monitor, the filter capacitors can be increased in size to reduce jitter. A value approximately 5 times the original value should eliminate jitter from this source.

The K-1008 can be coaxed into a 50Hz vertical rate simply by reducing the system clock rate from 1.0mHz to 833.33kHz. The phase locked loop on the Visible Memory will have to be adjusted to lock into the new clock rate. A disadvantage besides the 16% reduction in system speed is the reduction of horizontal sweep frequency to 13kHz. This frequency reduction results in a louder horizontal squeal and an increase in raster width. The latter can be rectified by adjusting the width coil or changing taps on the flyback transformer.

Another possibility is actual modification of the vertical freqency divider on the Visible Memory. This requires the addition of a 74LS21 IC, some etch cuts, and some jumper wires. The marked-up schematic on the next page shows the modifications and a list of instructions. With these modifications, the number of non-interlaced scan lines is increased to 312 and the vertical sweep frequency is reduced to 50.08Hz. The display format remains the same at 320 dots wide by 200 lines high however. With this simple modification the vertical sync width is greatly increased from .25MS to 3.58MS. This should not harm anything but may make the vertical sweep unstable unless the vertical hold control on the monitor is adjusted. Also the image portion of the raster may be shifted down somewhat on the screen but should still be completely visible.

50Hz Vertical Sweep Modification Instructions

___ 1. Cut trace running from U31-3 to U46-1

___ 2. Cut trace running from U31-3 to U32-2

___ 3. Cut trace running from U47-1 to U46-12

___ 4. Obtain a known good 74LS21 dual 4-input AND gate and glue it upsidedown on the top of the board between U47 and U32. Alternatively it may be mounted on a piece of perf-board mounted on the back edge of the VM board close to the video output jack.

___ 5. Run a wire from U31-1 to pin 1 on the new IC (Rember that the added IC is mounted upsidedown so the 1-7 and 8-14 pin rows will be flipped.)

___ 6. Run a wire from U32-10 to pin 2 on the new IC

___ 7. Run a wire from U32-11 to pin 4 on the new IC

___ 8. Run a wire from U32-6 to pin 5 on the new IC

___ 9. Run a wire from U46-12 to pins 13 and 12 on the new IC

___ 10. Run a wire from U45-7 to pins 10 and 9 on the new IC

___ 11. Run a wire from pin 8 on the new IC to U47-1

___ 12. Run a wire from pin 6 on the new IC to U46-1

___ 13. Run a wire from pin 6 on the new IC to U32-2

___ 14. Run a wire from U47-7 to pin 7 on the new IC

___ 15. Run a wire from U32-14 to pin 14 on the new IC

50Hz Principles of Operation

The modification outlined above replaces a 2 input AND gate with a 4 input AND gate and converts a 4 input NAND gate to a 5 input NAND gate.

In 60HZ operation U31-3 detects the coincidence of vertical retrace (part of U45) and the accumulation of 4 counts in the vertical divider. It then generates a reset signal which clears retrace and the divider. Pin 6 of the added IC simply allows the accumulation of 56 counts before reset occurs thus giving an overall divison ratio of 256+56=312 in the vertical section. Note that vertical sync is now 56 horizontal periods long.

The other half of U45 defines the 200 scan lines used to form the image. The image is started when the vertical divider reaches count 24 and is stopped when it reaches 224. In 60Hz operation there is no need to factor in vertical retrace since the divider never reaches 24 during retrace. This is no longer true with the 50Hz modification. Therefore pin 8 of the added IC factors in the retrace flip-flop state to prevent premature initiation of the image.